REQUESTED AMENDMENTS TO THE CLAIMS

Applicants respectfully request entry of the following cancellation of claims 3, 54, 55, 57 and 63 without prejudice or disclaimer to resubmission in a divisional or continuation application, as reflected in the following Listing of Claims, which is intended to replace all prior versions and Listings of Claims in the application:

1. **(Cancelled)**

2. **(Previously presented)** A chip comprising:

at least two processing units with separate memories and separate busses, wherein said at least two processing units exchange data therebetween by transferring said data between said memories;

at least one first in first out (FIFO) unit to transfer said data between said busses;

at least one first direct memory access (DMA) channel to transfer said data from one of said memories to said at least one FIFO unit; and

at least one second DMA channel to transfer said data from said at least one FIFO unit to another of said memories.

3. **(Canceled)**

4. **(Previously presented)** A chip according to claim 2 wherein said processing units are central processing units (CPUs).

5. **(Previously presented)** A chip according to claim 2 and further comprising at least two asynchronous clocks to control said at least two processing units.

6. **(Previously presented)** A chip according to claim 2 wherein one of said processing units is to process media access control (MAC) commands and another of said processing units is to process physical layer device (PHY) commands of a networking protocol.

7-25. **(Cancelled)**

26. **(Previously presented)** A chip according to claim 2 wherein said memories are random access memories (RAMs).

27. **(Previously presented)** A chip according to claim 2 and further comprising a common register accessible by said processing units to act as a channel of communication by which said processing units are to coordinate exchange of said data between them.

28-35. **(Cancelled)**

36. **(Previously presented)** A method for transferring data between processing units comprising:

sending data from a first processing unit embedded on a chip to a second processing unit embedded on said chip by establishing a first direct memory access (DMA) channel to a first in first out (FIFO) unit from a first memory directly accessible only by said first processing unit, and a second DMA channel from said FIFO unit to a second memory directly accessible only by said second processing unit.

37. **(Previously presented)** A method according to claim 36, wherein operation of said first DMA channel comprises any of the actions selected from the group consisting of:

transferring data from said first memory to said FIFO unit on request by said first processing unit;

waiting until said FIFO unit is not full before transferring each row of said data; and

notifying said first processing unit when all of said data has been transferred to said FIFO unit.

38. **(Previously presented)** A method according to claim 36, wherein operation of said second DMA channel comprises any of the actions selected from the group consisting of:

transferring data from said FIFO to said second memory on request by said second processing unit;

waiting until said FIFO unit is not empty before transferring each row of said data; and

notifying said second processing unit when all of said data has been transferred to said second memory.

39. **(Cancelled)**

40. **(Previously presented)** A method according to claim 36 wherein said first processing unit and said second processing unit are CPUs.

41. **(Previously presented)** A method according to claim 36 wherein said first memory and said second memory are RAMs.

42-55. **(Cancelled)**

56. **(Previously presented)** A device including a chip wherein said chip comprises:

at least two processing units with separate memories and separate busses, wherein said at least two processing units exchange data therebetween by transferring said data between said memories;

at least one first in first out (FIFO) unit to transfer said data between said busses;

at least one first direct memory access (DMA) channel to transfer said data from one of said memories to said at least one FIFO unit; and

at least one second DMA channel to transfer said data from said at least one FIFO unit to another of said memories.

57. **(Canceled)**

58. **(Previously presented)** A device according to claim 56 wherein said processing units are central processing units (CPUs).

59. **(Previously presented)** A device according to claim 56 wherein said chip further comprises at least two asynchronous clocks to control said at least two processing units.

60. **(Previously presented)** A device according to claim 56 wherein one of said processing units is to process media access control (MAC) commands and another of said processing units is to process physical layer device (PHY) commands of a networking protocol.

61. **(Previously presented)** A device according to claim 56 wherein said memories are random access memories (RAMs).

62. **(Previously presented)** A device according to claim 56 wherein said chip further comprises a common register accessible by said processing units to act as a channel of communication by which said processing units are to coordinate exchange of said data therebetween.

63. **(Canceled)**.